REMARKS/ARGUMENTS

Reconsideration is respectfully requested.

Claims 14-15 were pending in the present application before this amendment.

The applicants respectfully **disagree**.

According to an embodiment of the present invention as disclosed in FIG. 4, for example, a plurality of dividers such as 400, 410, 420, 430, and possibly more are connected in series. As the input signal S1 is processed through each divider, the frequency of S1 is divided into 1/2 (as in FIG. 4, but it should considered as to be within the scope of the present invention that a different ratio is also possible) at each stage, ie.e, A=(1/2)S1, B=(1/4)S1, C=(1/8)S1, and D=(1/16)S1. Then, the power down controller by utilizing two transmission gates 510, 520 in an embodiment shown in FIG. 4 to select the one of the signals A, B, C, D as the output signal S3 depending on the control signal CKE, which is representative of the power down mode. In the example according to the embodiment shown in FIG. 4, the clock divider is constructed such that the signal C (i.e., (1/8)S1) is wired to be connected to the transmission gate 510 (comprising a PMOS and a NMOS) and the signal D (i.e., (1/16)S1) is wired to be connected to the transmission gate 520.

To better clarify this aspect of the present invention, claim 14 has been amended to recite as follows:

> –a delay locked loop (DLL) having a clock divider **comprising a plurality of clock signal dividers connected in series**,
>
> –a power down controller for determining a power down condition based at least on a predetermined state of a clock enable signal inputted to the DLL,

--wherein the clock divider outputs a first clock signal **being one of the output signals of the clock signal dividers excluding the last clock signal divider of the series** when the synchronous memory device is in the power down condition,

--wherein the clock divider outputs a second clock signal **being an output signal of the last clock signal divider of the series** when the synchronous memory device is in a non-power down condition, and

--wherein a frequency of the first clock signal is lower than that of the second clock signal.--

This is not taught or suggested anywhere in Fujieda or Muraki, whether these two references are considered individually or in combination. As clearly shown in Fujieda FIG. 27 and described in Fujieda col. 16, line 45 to col. 17, line 15, Fujieda's frequency dividing ration setting part 53 outputs a "frequency dividing ratio setting signal" of "low" (see col. 17, lines 4-8) or "high" (see col. 17, lines 9-14) to **select** a set two signals "X" and "Z" (which is a dummy signal) that are generated from one of the two **discrete** frequency dividers 36 or 38 (that is, **not** connected in series as claimed). This has nothing to do with saving power consumption in Fujieda.

The examiner is respectfully referred to the specification page 6, lines 9-17, which describes the problems of the prior art solved by the present invention:

> "Accordingly, even in the case of a power-down mode in which the power consumption of the memory device is reduced, the output waveform of the clock divider becomes the same as that in a non-power down mode of the memory device. For this reason, the DLL circuit consumes the same amount of current as that in the non-power-down mode even though the memory device is in the power down-mode."

Fujieda's example circuit as shown in FIG. 27 **cannot** provide these power saving advantages as claimed since one of the two frequency dividers 36 and 38 will **always** output the predefined set of output signals "X" and "Z" depending on the signal from the

frequency dividing ratio setting part 53. That is, nowhere in Fujieda teaches or suggests a frequency divider that is capable of outputting a different frequency output signal depending on a control signal indicative of power savings mode.

Therefore, even if Fujieda and/or Muraki are considered individually or in combination, not all limitations of claim 14 is taught or suggested.

Further, MPEP §2143.01 requires that there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference to combine the reference teaching. That is, the mere fact that the teachings of the prior art **can** be modified or combined does **not** establish a motivation or suggestion to combine and make the resultant combination prima facie obvious. The suggestion or motivation to combine references must come from the cited prior art references, either explicitly or implicitly. MPEP §2143.01. There is **nothing** explicit or implicit in Fujieda that each of the frequency divider 36 or the frequency divider 38 is capable of generating a different frequency signal depending on a control signal form the frequency dividing ratio part 53. Further, there is **nothing** explicit or implicit in Fujieda that its circuit in 27 or anywhere else is capable of being utilized for power savings in a DLL circuit. In other words, Fujieda not only lacks to teach the claimed limitations of claim 14 but also fails to provide the required teaching or suggestion in the reference itself to establish adequately the desirability of Fujieda's teachings to apply for purposes of reducing power consumption.

The applicants respectfully submit that the conclusive statement of obviousness in the office action that FIG. 24 of Fujieda can be applied in power consumption savings

in a DLL is based on an impermissible presumption. The applicants' response to such a conclusive statement of obviousness is that the basis for improperly finding the presently claimed invention obvious appears to be the teaching found in this application, and not in the prior art. Thus, the obviousness rejection in the office action improperly relies on the **impermissible hindsight reasoning**, because the rejection would not be obvious absent the applicants' disclosure in this application that discloses the claimed hiding layer that is transferable to a different medium in presence of heat. (See 37 C.F.R. § 1.104(c)(2).) According to MPEP §2142, the hindsight reasoning based on the applicants' own disclosure is not permitted. Knowledge of applicants' disclosure must be set aside. The examiner must step back in time to when the invention was unknown and just before it was made. Only the fact gleaned from the prior art may be used.

Therefore, issuance of Notice of Allowance is respectfully requested. Should the examiner have any remaining questions or concerns, the examiner is encouraged to contact the undersigned attorney by telephone to expeditiously resolve such concerns.

Respectfully submitted,

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